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09/388,857	09/01/1999	LUAN C. TRAN	MI22-878	4528

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/388,857	TRAN, LUAN C.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,51-74 and 86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,51-74 and 86* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 54-56, 58-62 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's amended claim language of claim 54 states:

"the transistors provided with the different threshold voltages without using separate channel implants;

performing separate channel implants common to the transistors to provide the different threshold voltages".

The claim language contradicts itself and the Examiner cannot ascertain the scope of the claim. Therefore claim 54 and its dependents are indefinite.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 and 51-74 and 86 are rejected under 35 U.S.C. 102(e) as being anticipated by Liaw et al ('276).

In reference to claim 1, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas (Col.1, lines: 60-68), with some widths being no greater than 1 um, at least two being different (Col.2, lines: 1-10);

forming a transistor gate line over the active areas to provide individual transistors, the transistors corresponding to the active areas having the different widths having different threshold voltages, (Col.3-4, lines: 65-2) wherein the transistor having different widths and voltages (Table 1, Fig.4), wherein a smaller of the different widths has a lower of the different threshold voltages (Fig.4 (L= w/o imp)); and

wherein the active areas having the different widths each comprise a width of less than one micron. (Fig.4 (L= w/o imp)).

In reference to claim 2, Liaw et al teaches wherein there is no separate channel implant (Table 1, Fig.4).

In reference to claim 3, Liaw et al teaches wherein all the widths are less than one micron (Fig.4).

In reference to claim 4, Liaw et al teaches wherein the threshold voltages are less than 2 volts (Table 1, Fig.4).

In reference to claim 5, Liaw et al teaches wherein the threshold voltages are less than one volt (Table 1, Fig.4).

In reference to claim 6, Liaw et al teaches wherein the widths are less than one micron and the threshold voltages are less than 2 v (Table 1, Fig.4).

In reference to claim 7, Liaw et al teaches wherein the widths are less than one micron and the threshold voltages are less than 1 v (Table 1, Fig.4).

In reference to claim 51, Liaw et al teaches wherein one active area width is greater than 1 um (Table 1, Fig.4).

In reference to claim 52, Liaw et al teaches wherein forming individual transistors comprises forming three individual transistors, a first of the three having a first Tv, a second of the three having a second Tv, greater than the first Tv and a third of the three having a third Tv greater than the second Tv (Table 1, Fig.4)

In reference to claim 53, Liaw et al teaches wherein forming individual transistors, a first of the three having a first Tv, a second of the three having a second Tv, greater than the

first Tv and a third of the three having a third Tv greater than the second Tv (Table 1, Fig.4), the three individual transistors being configured to be coupled in parallel (Fig.3B).

In reference to claim 54, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas (Col.1, lines: 60-68), with some widths being no greater than 1 um, at least two being different (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different threshold voltages (Table 1, Fig.4), the transistors being provided with different threshold voltages without using a separate channel implant (Table 1, Fig.4).

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Table 1, Fig.4) wherein a smaller of the different widths has a lower of the different threshold voltages (Fig.4 (L= w/o imp)).

In reference to claim 55, Liaw et al teaches wherein the higher TV has an active area greater than 1 um (Table 1, Fig.4).

In reference to claim 56, Liaw et al teaches wherein the higher TV has an active area less than 1 um (Table 1, Fig.4).

In reference to claim 57, Liaw et al teaches wherein one common channel implant is conducted (Col.3, lines: 35-40).

In reference to claim 58, Liaw et al teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.3B).

In reference to claim 59, Liaw et al teaches wherein the gate line comprises a common gate line and the Ts are parallel (Fig. 3B).

In reference to claim 60, Liaw et al teaches wherein the TV are less than 1 V(Table 1, Fig.4).

In reference to claim 61, Liaw et al teaches wherein the widths are less than 1 um, and the TV are less than 2 V (Table 1, Fig.4).

In reference to claim 62, Liaw et al teaches wherein the widths are less than 1um and the TV are less than 1 V (Table 1, Fig.4).

In reference to claim 63, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas (Col.1, lines: 60-68), with some widths being no greater than 1 um, at least two being different (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different threshold voltages (Table 1, Fig.4), the transistors being provided with different widths having different threshold voltages without using a separate channel implant (Table 1, Fig.4),wherein the different threshold voltages are each less than 2 volts (Table 1, Fig.4)

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Table 1, Fig.4) wherein a smaller of the different widths has a lower of the different threshold voltages (Fig.4 (L= w/o imp)).

In reference to claim 64, Liaw et al teaches wherein the two widths are less than 1 um (Table 1, Fig.4).

In reference to claim 65, Liaw et al teaches wherein the TV are less than 1 v (Table 1, Fig.4)..

In reference to claim 66 Liaw et al teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Table 1, Fig.4).

In reference to claim 67, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define a plurality of active areas having widths over the substrate (Col.1,

lines: 60-68), with at least two of the widths being different and at least one of the plurality of widths being no greater than 1 um, (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different threshold voltages (Table 1, Fig.4), the transistors being provided with different threshold voltages without using a separate channel implant (Table 1, Fig.4), wherein the gate line comprises forming a gate line over the plurality of active areas, the transistor formed in an electrically parallel configuration (Fig.3B); and wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Table 1, Fig.4) wherein a smaller of the different widths has a lower of the different threshold voltages (Fig.4 (L= w/o imp)).

In reference to claim 68, Liaw et al teaches wherein the higher TV has an active area greater than 1 um (Table 1, Fig.4).

In reference to claim 69, Liaw et al teaches wherein the higher TV has an active area less than 1 um (Table 1, Fig.4).

In reference to claim 70, Liaw et al teaches wherein one common channel implant is conducted (Col.3, lines: 35-40).

In reference to claim 71, Liaw et al teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.3B).

In reference to claim 72, Liaw et al teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Table 1, Fig.4).

In reference to claim 73, Liaw et al teaches wherein the threshold voltages are less than 2 volts (Table 1, Fig.4).

In reference to claim 74, Liaw et al teaches wherein forming individual transistors, a first of the three having a first Tv, a second of the three having a second Tv, greater than the first Tv and a third of the three having a third Tv greater than the second Tv (Table 1, Fig.4), the three individual transistors being configured to be coupled in parallel (Fig.3B).

In reference to claim 86, wherein the transistor having a higher of the different threshold voltages comprises a larger of the different widths (Fig.4 (L=w/I imp).

Response to Arguments

Applicant's arguments filed 1/03/05 have been fully considered but they are not persuasive. Applicant argues that Liaw fails to teach more than one transistor having a width less than 1 micron- Liaw teaches four transistors each having a width less than one micron (Fig.4). Claim 54 is indefinite as explained above. Applicant argues that the channel width are not the active area widths as claimed however, as the Examiner has

outlined in previous responses to this same argument, this is unpersuasive. Lastly, Applicant argues that Liaw fails to teach the transistors are formed in an electrically parallel configuration, however, the gate line electrically connects the transistors in parallel as demonstrated in Fig.3B.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMS

03/05/05